Offline Current Mode PWM Controller with Programmable OTP/OVP

FEATURES

- **DCM and CCM Operation**
- **±1% CV Regulation**
- **Meet 6th Energy Star Requirement**
- **Less than 75mW Standby Power**
- **Fixed 65kHz Switching Frequency**
- **Green Mode and Burst Mode Control**
- **Very Low Startup and Operation Current**
- **Built-in Frequency Shuffling to Reduce EMI**
- **Built-in Current Mode Control with Internal Slope Compensation**
- **Built-in Protections with Auto Recovery:**
  - **VDD Under Voltage Lockout (UVLO)**
  - **VDD Over Voltage Protection (OVP)**
  - **CS Over Voltage Protection (CS OVP)**
  - **On-Chip Thermal Shutdown (OTP)**
  - **Programmable External Thermal Shutdown (OTP)**
  - **Cycle-by-Cycle Current Limiting**
  - **Over Load Protection (OLP)**
  - **Leading Edge Blanking (LEB)**
  - **CS Pin Float Protection**
- **Available with SOT23-6 Package**

APPLICATIONS

- **Charger and Adapter**
- **Motor Driver Power Supply**

GENERAL DESCRIPTION

KP201ALG is a high performance current mode PWM controller applied for offline flyback converter applications.

In KP201ALG, PWM switching frequency with shuffling is fixed to 65 kHz and is trimmed to tight range. The IC has built-in green and burst mode control for light and no load condition, which meet 6th energy star requirement and achieve less than 75mW standby power.

KP201ALG integrates functions and protections of Under Voltage Lockout (UVLO), VDD Over Voltage Protection (VDD OVP), CS Over Voltage Protection (CS OVP), Cycle-by-cycle Current Limiting (OCP), Short circuit protection (SCP), Over Load Protection (OLP), On-Chip Thermal Shutdown (OTP), Programmable External Thermal Shutdown (OTP), Soft Start, VDD clamping and CS Pin Float Protection, etc.

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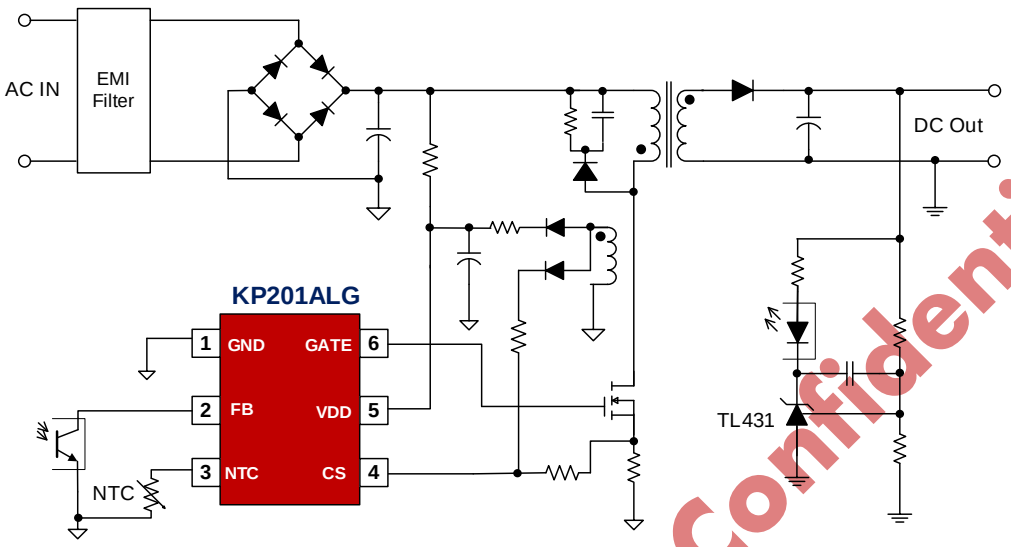
TYPICAL APPLICATION CIRCUIT



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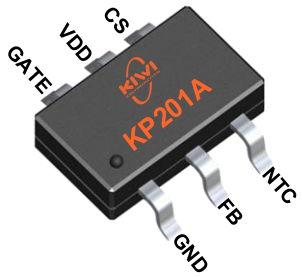
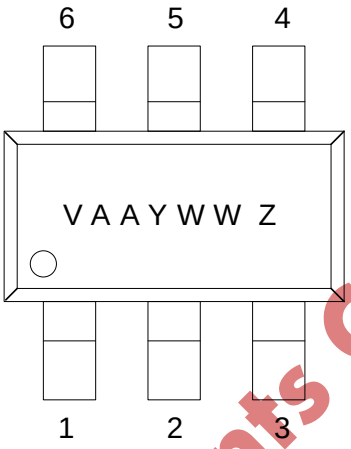
Pin Configuration



SOT23-6

Marking Information



VAA: KP201A
Y: Year Code
WW: Week Code, 01-52
Z: Serial Number, 1-9 or A-Z

SOT23-6

Pin Description

Pin Number	Pin Name	I/O	Description
1	GND	P	The ground of the IC
2	FB	I	Feedback pin. The loop regulation is achieved by connecting a photo-coupler to this pin. PWM duty cycle is determined by this pin voltage and the current sense signal at Pin 4
3	NTC	I	External programmable OTP pin
4	CS	I	Current sense input and CS OVP pin
5	VDD	P	IC power supply pin
6	GATE	O	Totem-pole gate driver output to drive the external MOSFET

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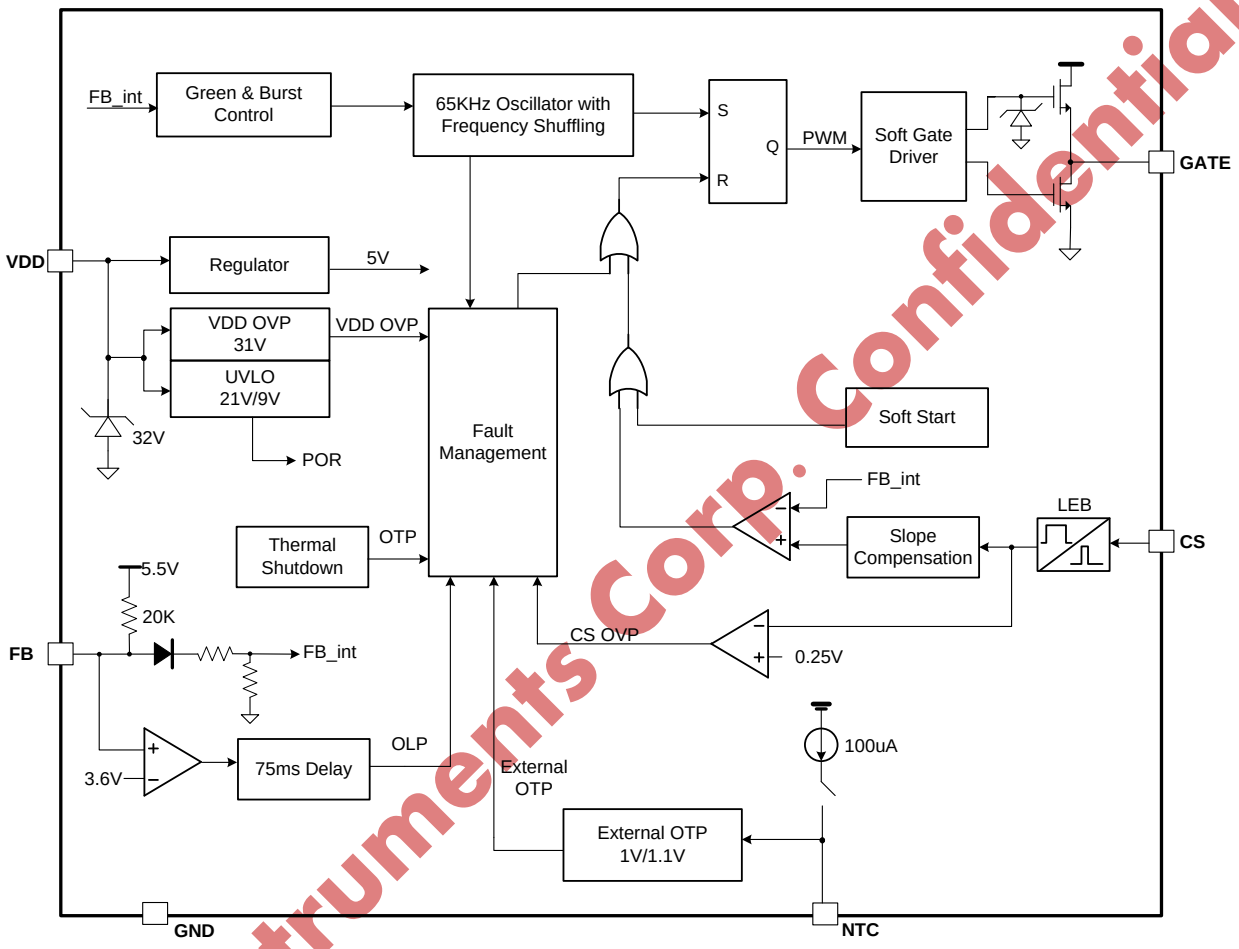
Ordering Information

Part Number	Description
KP201ALGA	SOT23-6, Halogen free, in T&R, 3000 Pcs/Reel

Block Diagram



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Absolute Maximum Ratings (Note 1)

Parameter	Value	Unit
VDD DC Supply Voltage	33	V
VDD DC Clamp Current	10	mA
FB, CS, NTC voltage range	-0.3 to 7	V
GATE voltage	20	V
Package Thermal Resistance---Junction to Ambient (SOT23-6L)	250	℃/W
Maximum Junction Temperature	175	℃
Storage Temperature Range	-65 to 150	℃
Lead Temperature (Soldering, 10sec.)	260	℃
ESD Capability, HBM (Human Body Model)	3	kV

Recommended Operation Conditions

Parameter	Value	Unit
Supply Voltage, VDD	10 to 28	V
Operating Ambient Temperature	-40 to 85	℃

Electrical Characteristics (TA= 25℃, VDD=18V, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage Section(VDD Pin)						
I_{VDD_st}	Start-up current into VDD pin			2	20	μA
I_{VDD_Op}	Operation Current	V_{FB}=3V,GATE=1nF		1.2	2	mA
$I_{VDD\_standby}$	Standby Current			0.6	1	mA
V_{DD_ON}	VDD Under Voltage Lockout Exit		19	21	21.5	V
V_{DD_OFF}	VDD Under Voltage Lockout Enter		8	9	10	V
V_{DD_OVP}	VDD OVP Threshold		29	31	33	V
V_{DD_Clamp}	VDD Zener Clamp Voltage	$I(V_{DD})$ = 7 mA	33	35	37	V
Feedback Input Section (FB Pin)						
V_{FB_Open}	FB Open Voltage			5.5		V
I_{FB_Short}	FB Short Circuit Current	Short FB Pin to GND, Measure Current		0.3		mA
Z_{FB_IN}	FB Input Impedance			20		KΩ
A_{CS}	PWM Gain	$\Delta V_{FB}/\Delta V_{CS}$		2.0		V/V
V_{skip}	FB Under Voltage GATE Clock is OFF			1.0		V
V_{TH_OLP}	Power Limiting FB Threshold Voltage			3.6		V
T_{D_OLP}	Power Limiting Debounce			75		ms

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	Time					
Current Sense Input Section (CS Pin)						
T_{LEB}	CS Input Leading Edge Blanking Time			250		ns
V_{cs_max}	Cycle-by-cycle Current limiting threshold		0.97	1.0	1.03	V
T_{D_OC}	Cycle-by-cycle Current limiting and Control Delay	GATE=1nF		70		ns
V_{CS_OVP}	CS Over Voltage Protection Threshold			250		mV
Oscillator Section						
F_{OSC}	Normal Oscillation Frequency		60	65	70	kHz
$\Delta F_{shuffle}/F_{OSC}$	Frequency Shuffling Range		-4		4	%
$T_{shuffle}$	Frequency Shuffling Period			32		ms
D_{MAX}	Maximum Switching Duty Cycle			66.7		%
F_{Burst}	Burst Mode Base Frequency			22		kHz
External OTP (NTC Pin)						
I_{OTP}	OTP Pin Source Current			100		μA
V_{OTP_Tr}	External OTP Trigger Voltage			1.0		V
V_{OTP_Re}	External OTP Recovery Voltage			1.1		V
On-Chip Thermal Shutdown						
T_{SD}	Thermal Shutdown	(Note 2)		165		˚C
T_{RC}	Thermal Recovery	(Note 2)		140		˚C
Driver Section (GATE Pin) (Note 3)						
V_{OL}	Output Low Level	Igate_sink=20mA			1	V
V_{OH}	Output High Level	Igate_source=20mA	7.5			V
V_{G_Clamp}	Output Clamp Voltage Level	VDD=24V		13		V
T_r	Output Rising Time	GATE=1nF		150		ns
T_f	Output Falling Time	GATE=1nF		60		ns

Note1. Stresses listed as the above "Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note2. Guaranteed by the Design.

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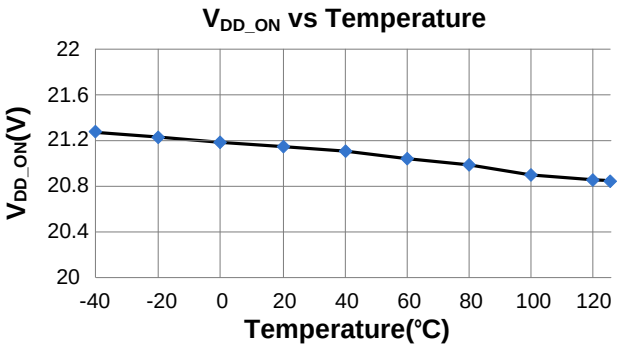
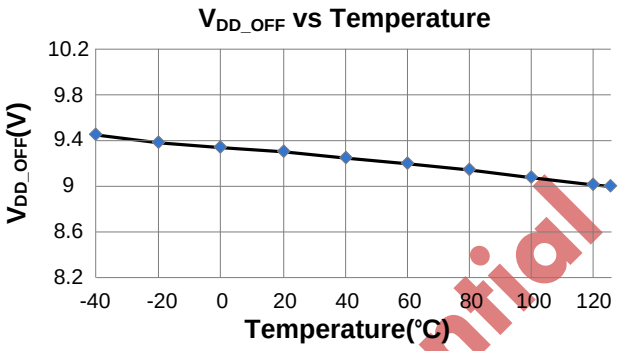
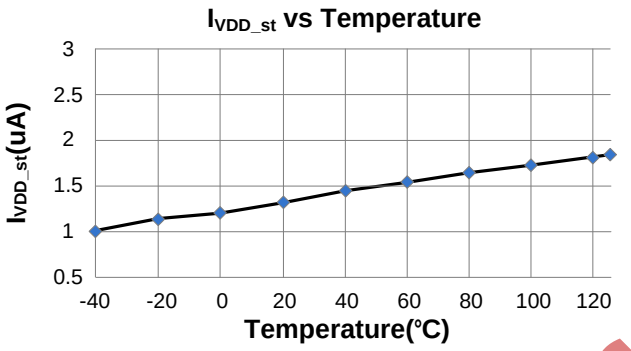
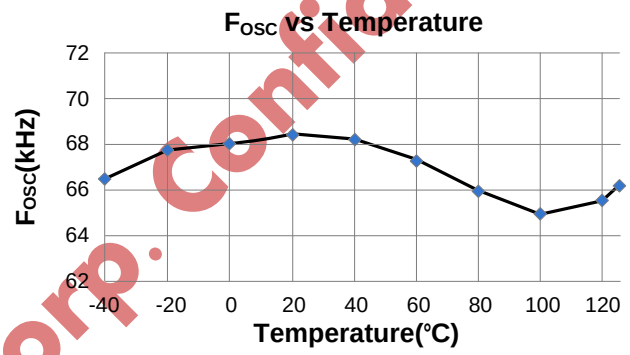
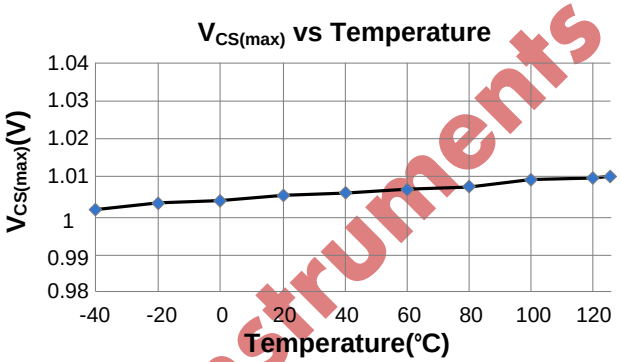
Characterization Plots











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Operation Description

KP201ALG is a high performance current mode PWM controller for offline flyback charger, motor driver power supply, and adapter applications. The IC can support CCM and DCM operation, which is suitable for isolated power supply design that requires CV regulation of the output.

System Start-Up Operation and IC Operation Current

Before the IC starts to work, it consumes only startup current (typically 2μA) which allows a large value startup resistor to be used to minimize the power loss and the current flowing through the startup resistor charges the VDD hold-up capacitor from the high voltage DC bus. When VDD reaches turn on threshold V_{DD_ON} (typically 21V), KP201ALG begins switching and the IC operation current increases to 1.2mA (typically). The hold-up capacitor continues to supply VDD before the auxiliary winding of the transformer takes the control of VDD voltage.

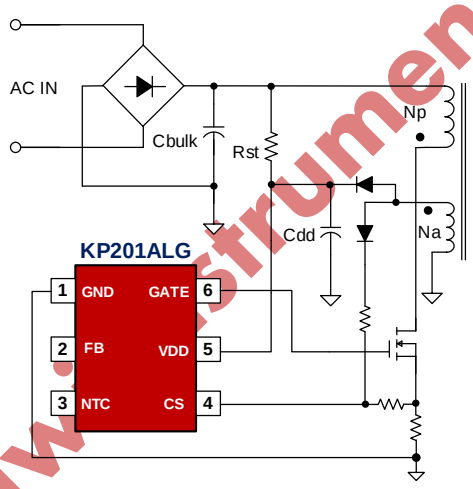

Fig.1

Oscillator with Frequency Shuffling

PWM switching frequency in KP201ALG is fixed to 65kHz and is trimmed to tight range. To improve system EMI performance, KP201ALG operates the system with 4% frequency shuffling around setting frequency.

Green Mode Operation

The main power dissipation at light/zero load in a switching mode power supply is from the switching loss which is proportional to the PWM switching frequency. To meet green mode requirement, it is necessary to reduce the switching cycles under such conditions either by skipping some switching pulses or by reducing the switching frequency.

Smooth Frequency Foldback

In KP201ALG, a proprietary “Smooth Frequency Foldback” function is integrated to foldback the PWM switching frequency when the load is light. Compared to the other frequency reduction implementations, this technique can reduce the PWM frequency smoothly without audible noise.

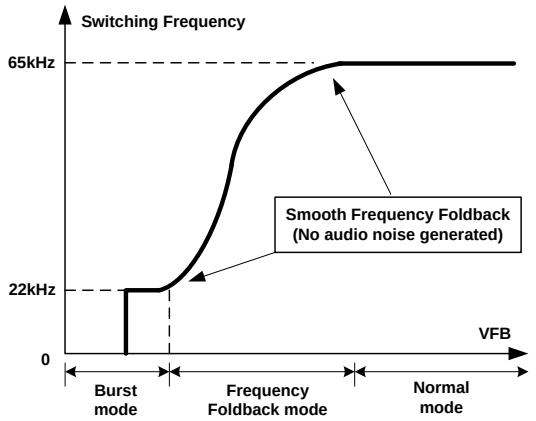

Fig.2

Burst Mode Control

When the load is very small, the system enters burst mode. When VFB drops below V_{skip}, KP201ALG stops switching and output voltage starts to drop (as shown in Fig.3), which causes the VFB to rise. Once VFB rises above V_{skip}, switching resumes. Burst mode control alternately enables and disables switching, thereby reducing switching loss in standby mode.

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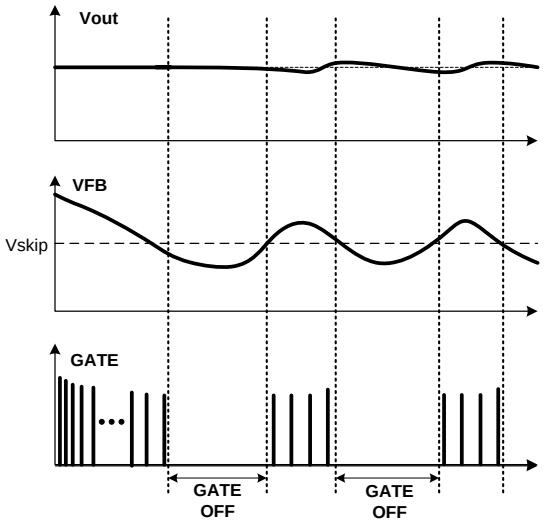

Fig.3

Built-in Slope Compensation

In the conventional application, the problem of the stability is a critical issue for current mode controlling when it operates in higher than 50% of the duty-cycle. In KP201ALG, the slope compensation circuit is integrated by adding voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM，prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Leading Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs across the sensing resistor. The spike is caused by primary side capacitance and secondary side rectifier reverse recovery. To avoid premature termination of the switching pulse, an internal leading edge blanking circuit is built in. During this blanking period (typically 250ns), the PWM comparator is disabled and cannot switch off the gate driver.

Thermal Shutdown (OTP)

KP201ALG integrates an external programmable OTP function. By connecting an NTC resistor between NTC pin and system ground, external OTP can be realized. NTC resistor value becomes lower when the ambient temperature rises. With the fixed internal current I_{OTP} (typically 100μA) flowing out from NTC pin, the voltage at NTC pin becomes lower at high temperature. When the sampled NTC voltage is below V_{OTP_Tr} (typically 1.0V) continuously in six switching cycles, system shuts down and enters auto recovery mode. When the sampled NTC voltage becomes higher than V_{OTP_Re} (typically 1.1V), system recovers from OTP state.

When the IC junction temperature is over 165 °C, the IC shuts down. Only when the IC temperature drops to 140 °C, IC restarts.

Soft Start

KP201ALG features an internal 2ms (typically) soft start that slowly increases the threshold of cycle-by-cycle current limiting comparator during startup sequence. It helps to prevent transformer saturation and reduce the stress on the secondary diode during startup. Every restart attempt is followed by a soft start activation.

Constant Power Limiting

A proprietary “Constant Power Limiting” block is integrated to achieve constant maximum output power capability over universal AC input range. Based on the duty cycle information, the IC generates OCP threshold according to a proprietary analog algorithm.

Over Load Protection (OLP)

If over load occurs, a fault is detected. If this fault is present for more than 75ms (typically), OLP is triggered and the IC experiences an auto-recovery mode protection as mentioned above. The 75ms

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delay time is to prevent the false trigger from the power-on and turn-off transient.

- **VDD Over Voltage Protection (OVP) and Zener Clamp**

When VDD voltage is higher than 31V (typically), the IC stops switching. This causes VDD to fall down to be lower than V_{DD_OFF} (typically 9V) and then the system restarts up again. An internal 35V (typically) zener clamp is integrated to prevent the IC from damage.

- **CS Over Voltage Protection**

KP201ALG integrates CS OVP function. CS pin is connected to auxiliary winding through a diode and resistor divider, which can sample the proportional output voltage signal. When CS voltage is higher than V_{CS_OVP} (typically 250mV) continuously in six switching cycles, CS OVP is triggered and enters auto recovery mode.

- **CS Pin Float Protection**

When VDD voltage is higher than V_{DD_ON} (typically 21V), IC firstly starts to check whether CS pin is floated. If CS pin is floated, switching is blocked and IC enters auto-recovery mode; otherwise, normal work begins. With this protection, system stability is enhanced.

- **Auto Recovery Mode Protection**

As shown in Fig.4, once a fault condition is detected, PWM switching stops. This causes VDD to fall because no power is delivered from the auxiliary winding. When VDD falls to V_{DD_OFF} (typically 9V), the protection is reset and the operating current reduces to the startup current, which causes VDD to rise. The system begins switching when VDD reaches to V_{DD_ON} (typically 21V). However, if the fault still exists, the system experiences the above-mentioned process. If the fault goes, the system resumes normal operation. In this manner, the auto restart can alternatively enable and disable the switching until the fault condition is disappeared.

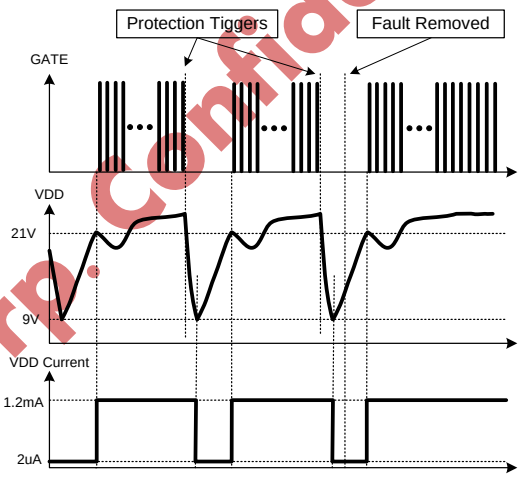

Fig.4

- **Soft Gate Driver**

The output stage of KP201ALG is a totem-pole gate driver with 400mA capability. Cross conduction is avoided to minimize heat dissipation, increase efficiency and enhance reliability. An internal 13V clamp is added for MOSFET gate protection at higher than expected VDD input. A soft driving waveform is implemented to minimize EMI.

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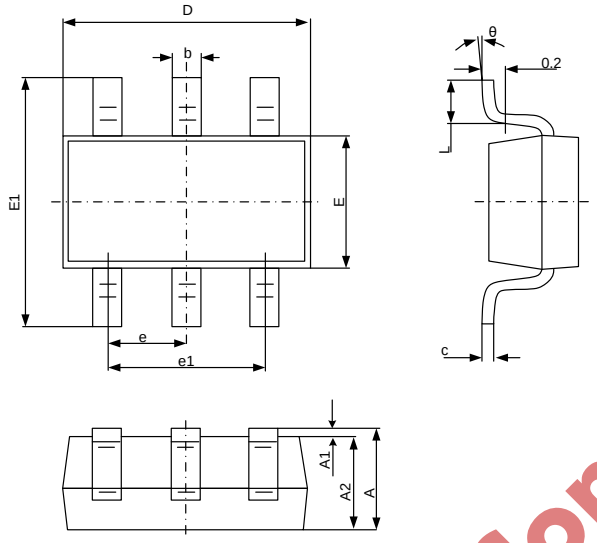
Package Dimension

SOT23-6



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	-	1.350	-	0.053
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.300	0.500	0.012	0.020
c	0.100	0.220	0.004	0.009
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.600	3.000	0.102	0.118
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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