# KP23132MSGA

## High Performance Primary Side Regulation CV/CC Power Switch With Single Failure Protections

## FEATURES

- **Built-in 800V High Voltage Power BJT**
- **Primary Side Regulation (PSR) Control with High Efficiency**
- **Single Failure Protections for power supply**
- **Multi-Mode PSR Control**
- **Fast Dynamic Response**
- **Optimized EMI Performance**
- **Audio Noise Free Operation**
- **±5% CC and CV Regulation**
- **Low Standby Power <30mW**
- **Programmable Cable Drop Compensation (CDC)**
- **Build in Protections:**
  - **Short Load Protection (SLP)**
  - **Cycle-by-Cycle Current Limiting (OCP)**
  - **On-Chip Thermal Shutdown (OTP)**
  - **VDD OVP & UVP & Clamp**
- **Available with SOP-8 Package**

## APPLICATIONS

- **Battery Chargers for Cellular Phones**
- **AC/DC Power Adapter**

## GENERAL DESCRIPTION

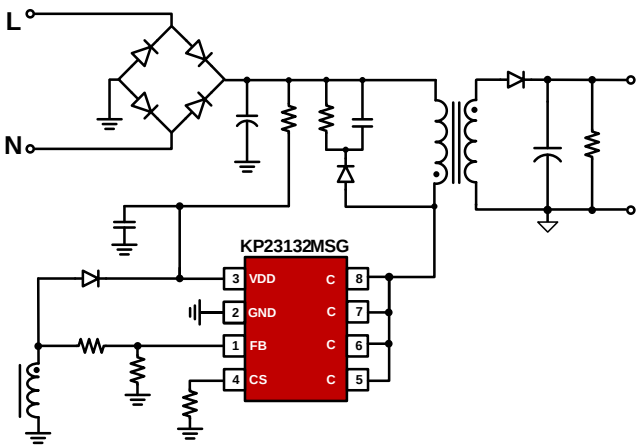
KP23132MSG is a high performance Primary Side Regulation (PSR) PWM power switch with high precision CV/CC control ideal for charger applications.

KP23132MSG can achieve audio noise free operation and fast dynamic response. The built-in Cable Drop Compensation (CDC) function can provide excellent CV performance.

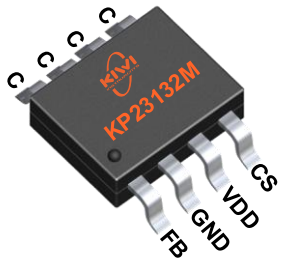
KP23132MSG integrates functions and protections of VDD Under Voltage Lockout (UVLO), VDD over Voltage Protection (VDD OVP), Cycle-by-cycle Current Limiting (OCP), Short Load Protection (SLP), On-Chip Thermal Shutdown, VDD Clamping, etc.

KP23132MSG also integrates single failure protections, including FB pull-up resistor open protection, FB pull-down resistor open protection, FB pull-down resistor short protection, output rectifier diode or SR open protection, output rectifier diode or SR short protection, transformer windings short protection, $R_{CS}$ open protection and IC GND pin open protection.

## TYPICAL APPLICATION CIRCUIT



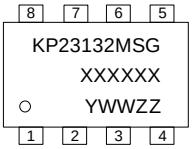
## Pin Configuration




**SOP-8**

## Marking Information

XXXXXX: Wafer Lot Code
Y: Year Code
WW: Week Code, 01-52
ZZ: Serial Number, 01-99 or A0-ZZ




**SOP-8**

## Typical Output Power Table(1)

| Part Number | 230VAC ± 15%(2) | 85-265VAC |
|---|---|---|
| | Adapter(3) | Adapter(3) |
| KP23132MSG | 15W | 12W |

**Note 1.** The Max. output power is limited by junction temperature.
**Note 2.**230VAC or 100/115VAC with voltage doublers.
**Note 3.**Typical continuous power in a non-ventilated enclosed adapter with sufficient drain pattern as a heat sink at 50℃ ambient.

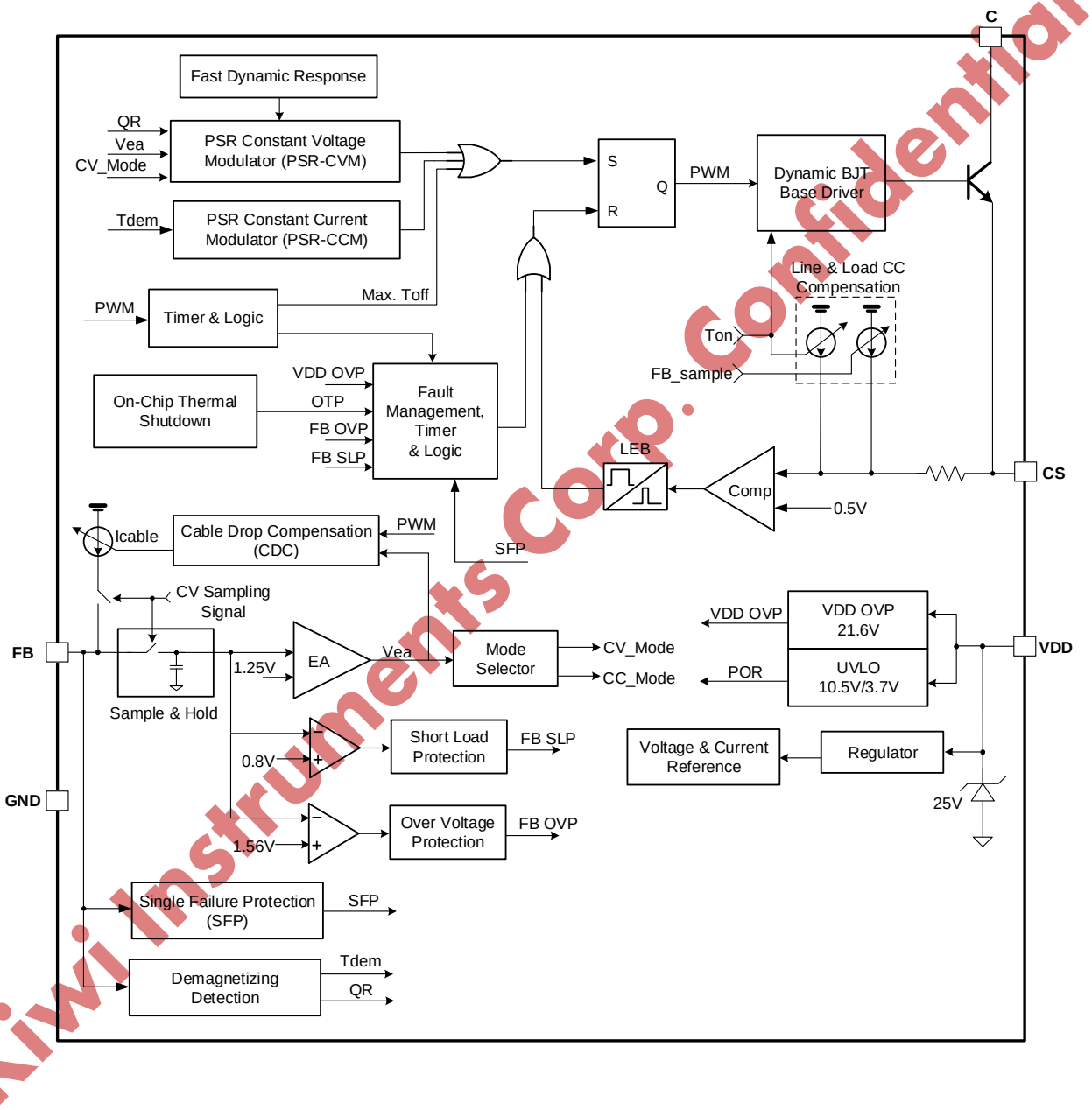
## Pin Description

| Pin Number | Pin Name | I/O | Description |
|---|---|---|---|
| 1 | FB | I | System feedback and Quasi-Resonant Detection Pin |
| 2 | GND | P | IC ground pin |
| 3 | VDD | P | IC Power supply pin |
| 4 | CS | I | Current Sense Input Pin |
| 5,6,7,8 | C | P | Internal power BJT collector pin |

## Ordering Information

| Part Number | Description |
|---|---|
| KP23132MSGA | SOP-8, Halogen free, in T&R,4000 Pcs/Reel |

## Block Diagram



## Absolute Maximum Ratings (Note 4)

| Parameter | Value | Unit |
|---|---|---|
| C Pin Voltage Range | -0.3 to 800 | V |
| VDD DC Supply Voltage | 25 | V |
| VDD DC Clamp Current | 10 | mA |
| CS Voltage Range | -0.3 to 7 | V |
| FB Voltage Range | -0.7 to 7 | V |
| Package Thermal Resistance---Junction to Case (SOP-8) | 80 | °C/W |
| Maximum Junction Temperature | 165 | °C |
| Storage Temperature Range | -40 to 165 | °C |
| Lead Temperature (Soldering, 10sec.) | 260 | °C |
| ESD Capability, HBM (Human Body Model) | 8 | kV |

## Recommended Operation Conditions

| Parameter | Value | Unit |
|---|---|---|
| Supply Voltage, VDD | 5 to 19 | V |
| Operating Ambient Temperature | -40 to 85 | °C |
| Maximum Switching Frequency @ Full Loading | 70 | kHz |
| Minimum Switching Frequency @ Full Loading | 35 | kHz |

## Electrical Characteristics ($T_A$= 25°C, VDD=16V, if not otherwise noted)

| Symbol | Parameter | Test Conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply Voltage Section (VDD Pin)** | | | | | | |
| $I_{VDD\_st}$ | Start-up current into VDD pin | VDD<$V_{DD\_ON}$ | 0.1 | 1.3 | 10 | μA |
| $I_{VDD\_Op}$ | Operation Current | | | 0.8 | 1.5 | mA |
| $I_{VDD\_standby}$ | Standby Current | | 0.1 | 0.13 | 0.2 | mA |
| $I_{OP\_Q}$ | Quiescent Current | | 0.13 | 0.18 | 0.2 | mA |
| $V_{DD\_ON}$ | VDD Under Voltage Lockout Exit | | 10 | 10.5 | 11 | V |
| $V_{DD\_OFF}$ | VDD Under Voltage Lockout Enter | | 3.6 | 3.7 | 3.8 | V |
| $V_{DD\_OVP}$ | VDD OVP Threshold | | 20.5 | 21.6 | 23 | V |
| $V_{DD\_Clamp}$ | VDD Zener Clamp Voltage | I($V_{DD}$) = 7 mA | 24.5 | 25 | 26.5 | V |
| **Control Function Section (FB Pin)** | | | | | | |
| $V_{FBREF}$ | Internal Error Amplifier (EA) Reference Input | | 1.24 | 1.25 | 1.26 | V |
| $V_{FB\_SLP}$ | Short Load Protection (SLP) Threshold | | | 0.8 | | V |

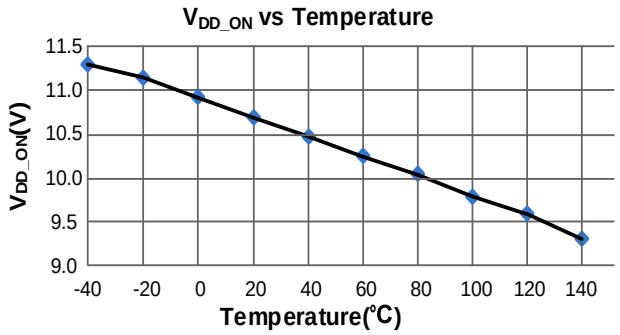
| | | | | | | |
|---|---|---|---|---|---|---|
| $V_{FB\_OVP}$ | FB Over Voltage Protection Threshold | | 1.48 | 1.56 | 1.64 | V |
| $T_{FB\_Short}$ | Short Load Protection (SLP) Debounce Time | (Note 5) | | 38 | | ms |
| $T_{FB\_OVP}$ | FB Over Voltage Protection Debounce Time | (Note 5) | | 3 | | Tsw |
| $V_{FB\_DEM}$ | Demagnetization Comparator Threshold (before start up) | Upper Threshold | | 30 | | mV |
| | | Lower Threshold | | -20 | | mV |
| | Demagnetization Comparator Threshold (after start up) | Upper Threshold | | 40 | | mV |
| | | Lower Threshold | | -100 | | mV |
| $T_{blank}$ | Leading Edge Blanking Time | CC Mode (Note5) | 3.6 | 4 | 4.4 | μs |
| | | CV Mode (Note5) | 1.8 | 2 | 2.2 | μs |
| $T_{on\_max}$ | Maximum ON time | (Note 5) | | 25 | | μs |
| $T_{off\_max}$ | Maximum OFF time | | | 6 | | ms |
| $I_{Cable\_max}$ | Maximum Cable Drop Compensation(CDC) Current | | | 15.6 | | μA |
| $T_{SW}/T_{DEM}$ | Ratio between Switching Period and Demagnetization Time in CC Mode | | | 2 | | |
| **Current Sense Input Section (CS Pin)** | | | | | | |
| $T_{LEB}$ | CS Input Leading Edge Blanking Time | | | 455 | | ns |
| $V_{cs(max)}$ | Current limiting threshold | | 496 | 499 | 504 | mV |
| $V_{cs(min)}$ | Current limiting threshold | | 215 | 231 | 245 | mV |
| $T_{D\_OC}$ | Over Current Detection and Control Delay | | | 100 | | ns |
| **On-Chip Thermal Shutdown** | | | | | | |
| $T_{SD}$ | Thermal Shutdown | (Note 5) | 150 | 155 | 160 | °C |
| $T_{RC}$ | Thermal Recovery | (Note 5) | 120 | 125 | 130 | °C |
| **Power BJT Section (C Pin)** | | | | | | |
| Ic | Maximum Collector Current | Continuous Current | 2.5 | | | A |
| | | Pulse Current | 10 | | | A |
| $V_{CE(sat)}$ | Collector-Emitter Saturation Voltage | $I_C$=0.5A | | 0.3 | | V |
| $h_{FE}$ | DC Current Gain | | 20 | | 30 | |
| $V_{CBO}$ | Collector-Base Breakdown Voltage | | 800 | | | V |

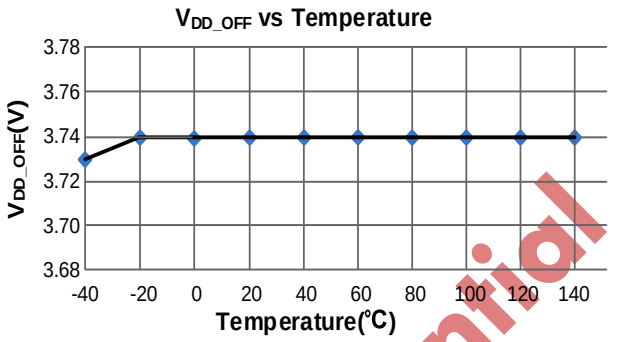


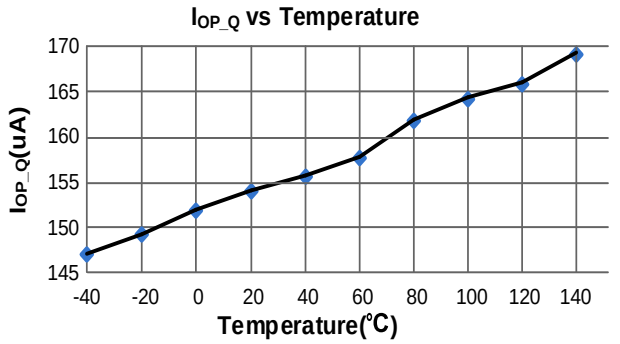
**Note 4.** Stresses listed as the above “Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.

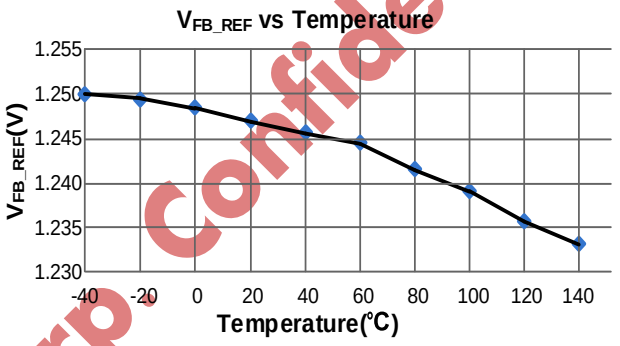
**Note 5.** Guaranteed by the Design.

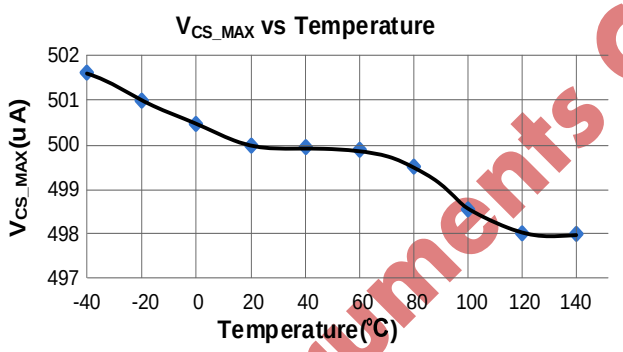
## Characterization Plots

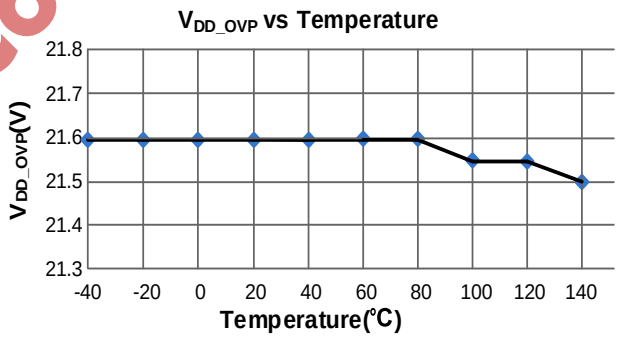


## Operation Description

KP23132MSG is a high performance, multi-mode, Primary Side Regulation (PSR)power switch. The built-in high precision CV/CC control with high level protection features makes it suitable for offline small power converter applications

### • System Start-Up Operation

Before the IC starts to work, it consumes only startup current (typically 1.3μA) which allows a large value startup resistor to be used to minimize the standby power loss. When VDD reaches turn-on voltage of 10.5V (typical), KP23132MSG begins switching and the IC operation current is increased to be 0.18mA (typical). The hold-up capacitor continues to supply VDD before the auxiliary winding of the transformer takes control.

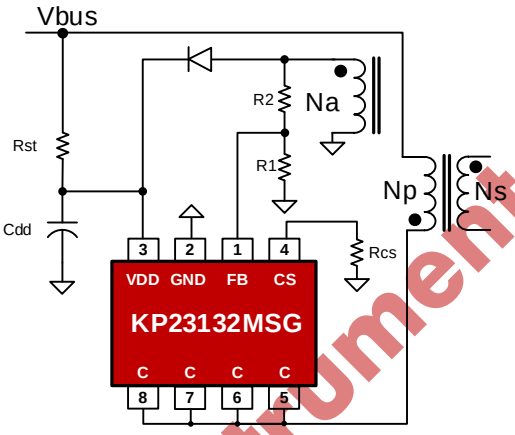



Fig.1

Once KP23132MSG enters very low frequency FM (Frequency Modulation) mode, the operating current is reduced to be 0.13mA typically, which helps to reduce the standby power loss.

### • PSR CV Modulation (PSR-CVM)

In Primary Side Regulation (PSR) control, the output voltage is sensed on the auxiliary winding during the transfer of transformer energy to the secondary. Fig.2 illustrates the timing waveform of CV sampling signal, demagnetization signal (DEM). When the CV sampling process is over, the internal sample/hold (S&H) circuit captures the error signal and amplifies it through the internal Error Amplifier (EA). The output of EA is sent to the PSR CV Modulator (PSR-CVM) for CV regulation. The internal reference voltage for EA is trimmed to 1.25V with high accuracy.

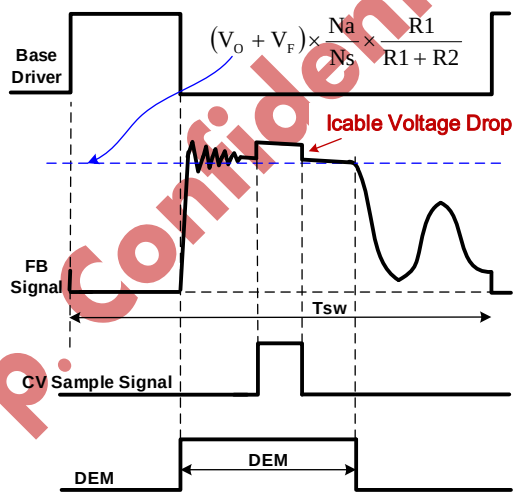



Fig.2

During the CV sampling process, an internal variable current source is flowing to FB pin for Cable Drop Compensation (CDC). Thus, there is a step at FB pin in the transformer demagnetization process, as shown in Fig.2. Fig.2 also illustrates the equation for “demagnetization plateau”,

$$V_{FB} = (V_O + V_F) \times \frac{Na}{Ns} \times \frac{R1}{R1+R2}$$

Where Vo and VF is the output voltage and diode forward voltage; R1 and R2 is the resistor divider connected from the auxiliary winding to FB Pin, Ns and Na is secondary winding and auxiliary winding respectively.

When heavy load condition, the Mode Selector (as shown in “**Block Diagram**”) based on EA

output will switch to CC Mode automatically.

- **PSR Constant Current Modulation (PSR-CCM)**

Timing information at the FB pin and current information at the CS pin allow accurate regulation of the secondary average current. The control law dictates that as power is increased in CV regulation and approaching CC regulation the primary peak current is at Ipp (max), as shown in Fig.3.

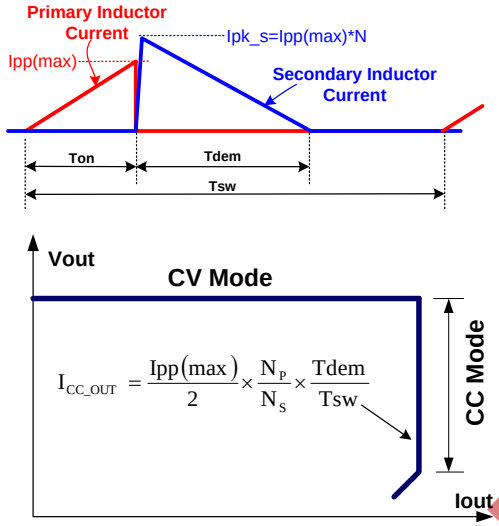



Fig.3

Referring to Fig.3 above, the primary peak current, transformer turns ratio, secondary demagnetization time (Tdem), and switching period (Tsw) determines the secondary average output current Iout. Ignoring leakage inductance effects, the equation for average output current is shown in Fig.3. When the average output current Iout reaches the regulation reference in the Primary Side Constant Current Modulator (PSR-CCM) block, the IC operates in pulse frequency modulation (PFM) mode to control the output current at any output voltage at or below the voltage regulation target as long as the auxiliary winding can keep VDD above the UVLO turn-off threshold.

In KP23132MSG, the ratio between Tdem and Tsw in CC mode is 1/2. Therefore, the average output current can be expressed as:

$$I_{CC\_OUT}(\text{mA}) \cong \frac{1}{4} \times N \times \frac{500\text{mV}}{\text{Rcs}(\Omega)}$$

In the equation above,

N----The turn ratio of primary side winding to secondary side winding.

Rcs--- the sensing resistor connected between the power BJT emitter to GND.

- **Multi-Mode Control in CV Mode**

To meet the tight requirement of averaged system efficiency and no-load power consumption, a hybrid of frequency modulation (FM) and amplitude modulation (AM) is adopted in KP23132MSG which is shown in the Fig 4.

Around the full load, the system operates in FM mode. When normal to light load conditions, the IC operates in FM+AM mode to achieve excellent regulation and high efficiency. When the system is near zero loading, the IC operates in FM again for standby power reduction. In this way, the no-load consumption can be less than 30mW.

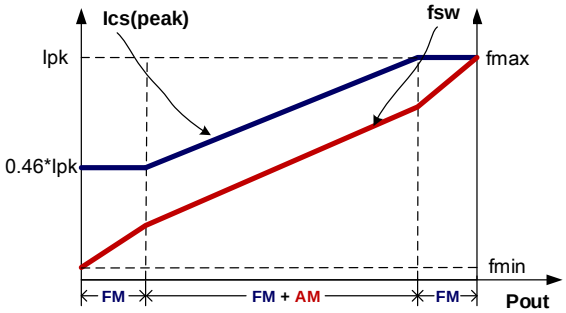



Fig.4

- **Cable Drop Compensation (CDC) in CV Mode**

In smart phone charger application, the battery is always connected to the adapter with a cable wire which can cause several percentages of voltage drop on the actual battery voltage. In KP23132MSG, an offset voltage is generated at FB pin by an internal current source (modulated by CDC block, as shown in Fig.5) flowing into the resistor divider. The current is proportional to the switching period; thus, it is inversely proportional to the output power Pout. Therefore, the drop due the cable loss can be compensated. As the load decreases from full loading to zero loading, the offset voltage at FB pin will increase. The percentage of maximum compensation is given by

$$\frac{\Delta V(\text{cable})}{\text{Vout}} \approx \frac{\text{Icable\_max} \times (\text{R1}//\text{R2})}{V_{\text{FB\_REF}}} \times 100\%$$

For example, R1=5KΩ, R2=40KΩ, The percentage of maximum compensation is given by:

$$\frac{\Delta V(\text{cable})}{\text{Vout}} \approx \frac{16u \times (40\text{k}//5\text{k})}{1.25} \times 100\% = 5.69\%$$

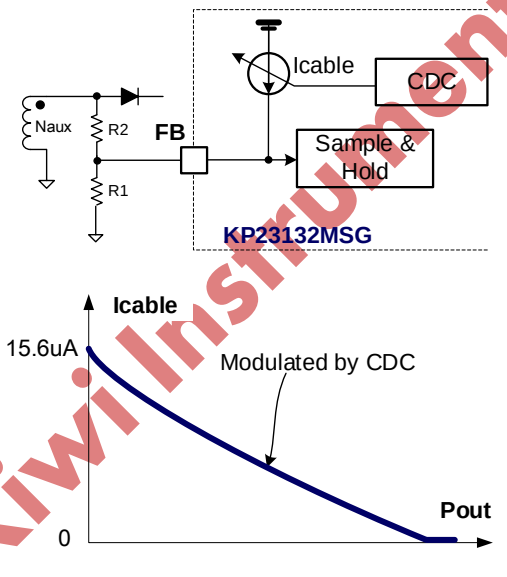



Fig.5

- **Fast Dynamic Response**

In KP23132MSG, the dynamic response performance is optimized to meet USB charge requirements.

- **Single Failure Protections for Power Supply**

KP23132MSG integrates single failure protections, including FB pull-up resistor open protection, FB pull-down resistor open protection, FB pull-down resistor short protection, output rectifier diode or SR open protection, output rectifier diode or SR short protection, transformer windings short protection, $R_{CS}$ open protection and IC GND pin open protection. This function can ensure there is no damage to IC and no over voltage of output.

- **On Chip Thermal Shutdown (OTP)**

When the IC temperature is over 160°C, the IC shuts down. Only when the IC temperature drops to 135°C, IC will restart.

- **Audio Noise Free Operation**

As mentioned above, the multi-mode CV control with a hybrid of FM and AM provides frequency modulation is used in CV mode. An internal current source flowing to CS pin makes CS peak voltage modulation realized. In KP23132MSG, the optimized combination of frequency modulation and CS peak voltage modulation algorithm can provide audio noise free operation from full loading to zero loading.

- **Dynamic BJT Base Drive**

KP23132MSG integrates a dynamic base drive control to optimize efficiency. The BJT base drive current is dynamically controlled according to the power supply load change. The higher the output power, the higher the based current.

- **Short Load Protection (FB SLP)**

In KP23132MSG, the output is sampled on FB pin

and then compared with a threshold of UVP (0.8V typically).

In KP23132MSG, when sensed FB voltage is below 0.8V and hold 38ms, the IC will enter into Short Load Protection (SLP) mode, in which the IC will enter into auto recovery protection mode.

- **FB Over Voltage Protection (FB OVP)**

In KP23132MSG, the output is sampled on FB pin and then compared with a threshold of OVP (1.56V typically).

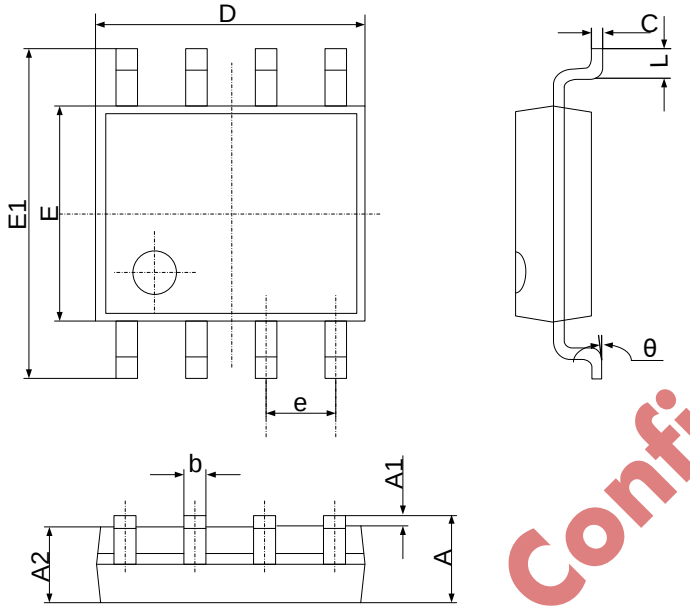
When sensed FB voltage is above 1.56V for more than 3 cycles, the IC will enter into Over Voltage Protection (OVP) mode, in which the IC will enter into auto recovery protection mode.

- **VDD Over Voltage Protection (OVP) and Zener Clamp**

When VDD voltage is higher than 21.6V (typical), the IC will stop switching. This will cause VDD fall down to be lower than $V_{DD\_OFF}$ (typical 3.7V) and then the system will restart up again. An internal 25V (typical) zener clamp is integrated to prevent the IC from damage.

## Package Dimension

**SOP-8**




| Symbol | Dimensions in Millimeters | | Dimensions in Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.350 | 1.550 | 0.053 | 0.061 |
| b | 0.330 | 0.510 | 0.013 | 0.020 |
| c | 0.170 | 0.250 | 0.006 | 0.010 |
| D | 4.700 | 5.100 | 0.185 | 0.200 |
| E | 3.800 | 4.000 | 0.150 | 0.157 |
| E1 | 5.800 | 6.200 | 0.228 | 0.244 |
| e | 1.270 (BSC) | | 0.050 (BSC) | |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0º | 8º | 0º | 8º |



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