PWM Dimmable APFC Buck LED Power Switch

FEATURES

- PWM Dimming
- 15mW Ultra low standby power
- Dimming depth <3%
- High PF Value >0.9
- Built-in Power Supply Circuit
- Internal 600V Power MOSFET
- No VDD, COMP Capacitor Design
- QR Operation Mode for High Efficiency
- High Output Current Accuracy< ± 3% @100% ILED
- Good Line and Load Regulation
- Built-in Protections:
  - Programmable Output Over Voltage Protection (OVP)
  - Cycle by Cycle Current Limit (OCP)
  - Leading Edge Blanking (LEB)
  - LED Open and Short Protection
  - Thermal Fold-back (OTP)
- Package Available with SOP-7

APPLICATIONS

- Low power intelligent bulb lamp

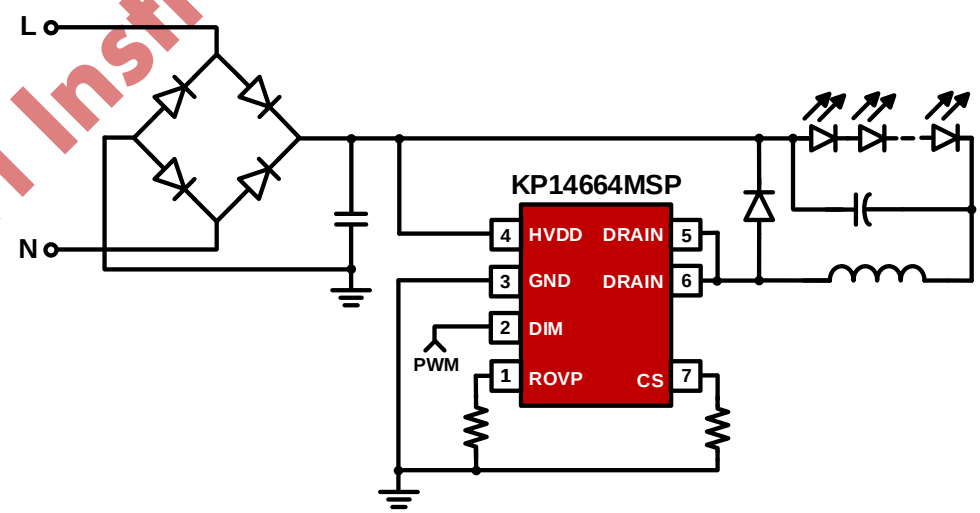
GENERAL DESCRIPTION

KP14664MSP is a family of highly integrated Constant Current LED power switch. The IC utilizes Quasi-Resonant (QR) Buck topology with active PFC control for high PF, low THD, and high efficiency.

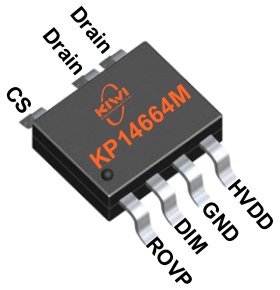
KP14664MSP integrates internal demagnetization detection circuit and 600V power MOSFET with high voltage startup, which eliminates auxiliary winding for power supply and demagnetization and simplifies the design and production cost of the system. The IC adopts accurate current sensing, close loop constant current control to achieve high precision CC control with excellent line and load regulation. KP14664MSP also integrates unique dimming technology to provide high precision PWM dimming.

KP14664MSP integrates functions and protections of Cycle-by-cycle Current Limiting (OCP), Thermal Fold-back (OTP), Output Over Voltage Protection (OVP), LED Open/Short Protection, etc.

TYPICAL APPLICATION CIRCUIT

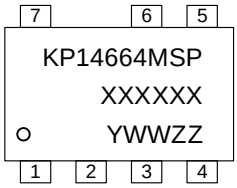


Pin Configuration



SOP-7

Marking Information



XXXXXX : Wafer Lot Code
Y : Year Code
WW : Week Code, 01-52
ZZ : Serial Number, 01-99 or A0-ZZ

SOP-7

Typical Output Power Table

Part Number	Package	Maximum Output Current (90-265Vac)	
		36V output	72V output
KP14664MSP	SOP-7	400mA	270mA

Note: Maximum output power is constrained by IC maximum Junction Temperature and determined by ambient temperature and PCB. The system actual maximum output power is determined by the test.

Pin Description

Pin Number	Pin Name	I/O	Description
1	ROVP	I	Output OVP adjustment pin. Connecting a resistor to GND can continuously adjust the OVP point. The OVP and output voltage of quick start finishing are proportional to ROVP resistance. ROVP pin cannot be floating or grounded. The recommended OVP is 1.4 ~ 1.6 times steady output voltage.
2	DIM	I	Output current regulating pin, receiving pulse signal input. When PWM pulse width is less than 1μs, IC will enter standby mode.
3	GND	P	IC Ground Reference Pin
4	HVDD	P	IC HV Supply Pin
5, 6	Drain	P	Internal power MOSFET Drain pin
7	CS	I	Internal power MOSFET Source and current sampling pin

Ordering Information

Part Number	Description
KP14664MSPA	SOP-7, Pb free in T&R, 4000 Pcs/Reel

Absolute Maximum Ratings (Note 1)

Parameter	Value	Unit
HVDD Voltage	-0.3 to 650	V
Drain Voltage	-0.3 to 600	V
CS, ROVP,DIM Voltage	-0.3 to 7	V
P_{Dmax}, Power dissipation @T_A=50°C (SOP-7) (Note2)	0.6	W
θ_{JA}, Thermal Resistance---Junction to Ambient (SOP-7) (Note2)	165	°C/W
Maximum Junction Temperature	150	°C
Storage Temperature Range	-65 to 150	°C
Lead Temperature (Soldering, 10sec.)	260	°C
ESD Capability, HBM (Human Body Model)	3	kV

Recommended Operation Conditions

Parameter	Value	Unit
Operating Junction Temperature	-40 to 125	°C

Electrical Characteristics (Ta = 25℃, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage Section (HVDD Pin)						
I_{HVDD_ST}	Start-up current into VDD pin	HVDD< $HVDD_{ON}$	0.8	1.4	2.0	mA
I_{HVDD_OP}	Operation Current	Fsw=7kHz	120	240	320	μA
I_{HVDD_STB}	Standby mode current		20	26	32	μA
$HVDD_{ON}$	HVDD Startup Voltage		13	15.5	17	V
$HVDD_{OFF}$	HVDD Under Voltage Lockout Enter		4.8	5.8	6.8	V
Timing Section						
T_{DEM_BLANK}	Demagnetization Detection blanking Time	(Note 3)	0.3	0.5	0.7	μs
T_{ON_MAX}	Maximum ON Time	(Note 3)	14	15.5	17	μs
T_{OFF_MAX}	Maximum OFF Time		100	140	160	μs
Current Sense Input Section (CS Pin)						
V_{CC_REF}	Internal Reference for CC Loop Regulation		180	185	190	mV

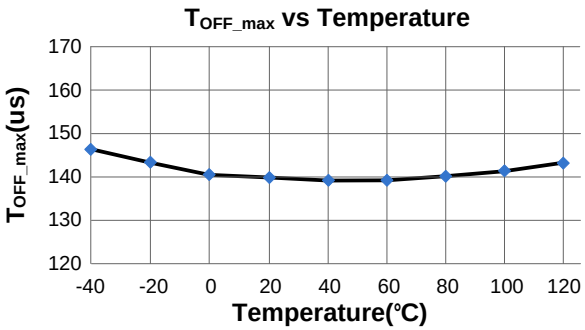
T_{LEB}	OCP Leading Edge Blanking Time			500		ns
V_{CS_MAX}	Current Limiting Threshold		1.4	1.5	1.6	V
T_{D_OC}	Over Current Detection and Control Delay			150		ns
Dimming Section (Dim Pin)						
V_{DIMH_th}	PWM Dimming High Level threshold		1.9	2	2.1	V
V_{DIML_th}	PWM Dimming Low Level threshold		0.4	0.5	0.6	V
$T_{DIM\_OFF\_L}$	PWM Dimming Off Threshold		0.8	1	1.2	μs
$T_{DIM\_OFF\_H}$	PWM Dimming Off Hysteresis		1.3	1.5	1.7	μs
F_{PWM_DIM}	PWM Frequency Range		0.6		10	kHz
Output Over Voltage Protection Section (ROVP Pin)						
I_{ROVP}	ROVP Pin Output Current			40		μA
Over Temperature Protection						
T_{OTP}	Thermal Foldback Trigger Point	(Note 3)		155		°C
Power MOSFET Section (Drain Pin)						
V_{BR}	Power MOSFET Drain Source Breakdown Voltage		600			V
R_{dson}	Static Drain-Source On Resistance	KP14664MSP		2.3		Ω

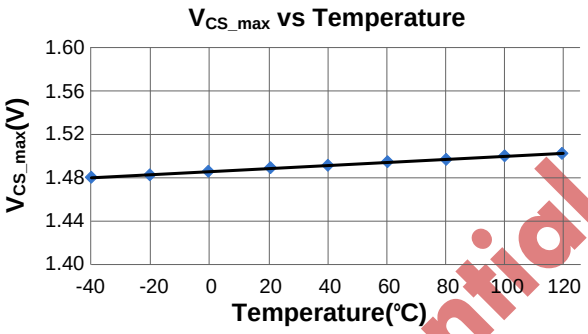
Note 1. Stresses listed as the above "Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.

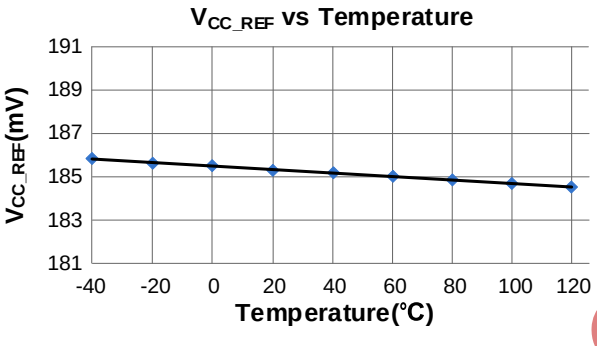
Note 2. Maximum power dissipation $P_{Dmax}= (T_{Jmax}-T_A)/\theta_{JA}$. As ambient temperature rises, P_{Dmax} will decrease.

Note 3. Guaranteed by the design.

Characterization Plots







Operation Description

KP14664MSP is a highly integrated power switch with constant current (CC) control for LED lighting applications. The IC utilizes Quasi-Resonant (QR) Buck topology with active PFC control for high PF, low THD, and high efficiency. KP14664MSP integrates internal loop compensation capacitor (COMP capacitor) and VDD capacitor and supports for non-auxiliary winding design. Output OVP voltage is continuously adjustable. The system cost can be minimized. At the same time, the IC also supports digital dimming.

● System Start-Up Operation

After system power up, a digital counter is enabled. When 64ms had been counted, IC starts to switch. There are two processes: 1. Quick start, IC works in fixed CS peak voltage state. Output voltage rises rapidly. Quick start will end when output voltage reaches 0.4 times OVP. 2. Constant current closed loop control with Ton increasing gradually until the output current rises to the set value.

● Constant Current (CC) Control

KP14664MSP samples the peak inductor current in each switching cycle to be as the CC loop feedback, and the high accurate output current can be realized with a high accurate current reference. The output current is determined by:

$$I_{LED}(mA)=\frac{V_{CC\_REF}}{R_{CS}}=\frac{185mV}{R_{CS}(\Omega)}$$

In the equation above,

R_{CS}--- the sensing resistor connected between CS and GND.

● PWM Dimming

KP14664MSP supports high precision PWM dimming. The relationship between IC internal current reference V_{cc_ref}, LED current I_{LED} and duty cycle D is as shown in Fig.1. There is a I_{LEDmin} which depends on T_{onmin}, inductor and input voltage.

When PWM pulse width is less than 1μs, IC stops switching, I_{LED} is 0 and IC enters standby mode; When increasing PWM pulse width to be over 1.5μs, I_{LED} increases to I_{LEDmin} from 0.

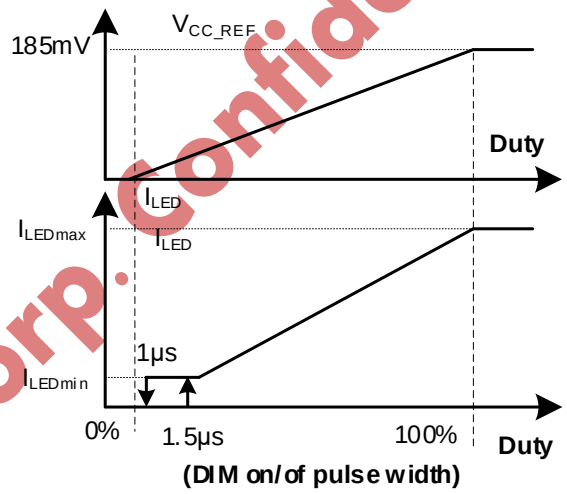


Fig. 1

● Leading Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs across the sensing resistor. The spike is caused by MOSFET parasitic capacitor and freewheeling rectifier reverse recovery. To avoid premature termination of the switching pulse, an internal leading-edge blanking circuit is built in. During this blanking period (500ns, typical), the PWM comparator is disabled and cannot switch off the gate driver.

● Demagnetization Detection

KP14664MSP integrates internal demagnetization detection circuit which eliminates the auxiliary winding and simplifies the design cost of the system.

Timing Control

In KP14664MSP, a minimum blanking time (typically 0.5μs) is implemented to suppress ringing when the power MOSFET is off. Meanwhile the maximum OFF time in KP14664MSP is typically 140μs.The chip also integrates maximum frequency clamping function (typically 125kHz) to achieve good EMI performance.

Output Over Voltage Protection (OVP)

KP14664MSP is integrated proprietary OVP control scheme, and the output over voltage can be programmed by the R_{OVP}. The output over voltage is determined by:

$$V_{OVP}(V) \approx \frac{13.2 \times L_P \times R_{OVP}}{R_{CS}}$$

where：

L_P---Inductance in H.

R_{CS}---current sense resistor in Ω

R_{OVP}---the resistor connected between ROVP and GND, in Ω.

Auto-Restart LED Open Protection

In the event of LED open circuit condition/output OVP protection, the IC enters auto-restart mode, wherein the power MOSFET is disabled and a digital counter is enabled. When 250ms had been counted, the IC will reset and start up the system again. However, if the fault still exists, the system will experience the above-mentioned process.

On Chip Thermal Fold-back (OTP)

KP14664MSP integrates thermal fold-back function. When the IC temperature is over 155°C, the system output regulation current is gradually reduced, as shown in Fig.2. Thus, the output power and thermal dissipation are also reduced. In this way, the system temperature is limited and system reliability is also improved.

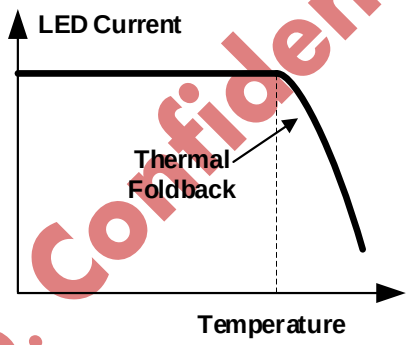


Fig.2

Soft Totem-Pole Gate Driver

KP14664MSP has a soft totem-pole gate driver with optimized EMI performance.

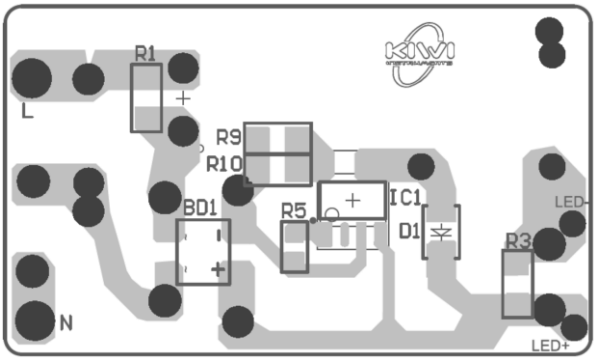
PCB Layout Guidelines

PCB layout is very important for reliable operation. Please follow guideline to optimize performance.

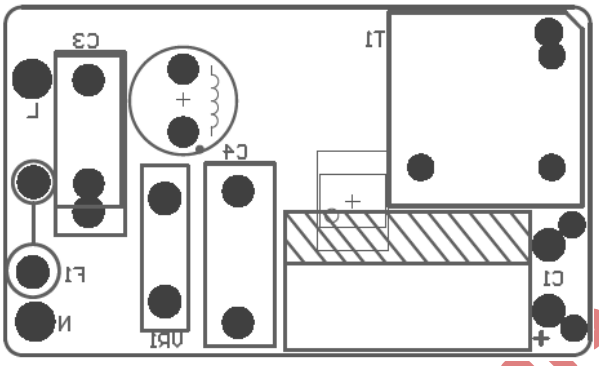
1. The area of main power switching loop should be as small as possible to reduce the EMI radiation, such as the inductor charging loop consisted of the EMI filter capacitor, output capacitor, inductor and IC; the inductor discharging loop consisted of the inductor, freewheeling diode and output capacitor.

2. Use single-point grounding. IC ground and other small signals ground should be connected to terminal ground point, the current sampling resistor ground. And the trace should be as short as possible.

3. Increase the copper area of the Drain pin to improve thermal performance. But too much copper area will worsen EMI performance.



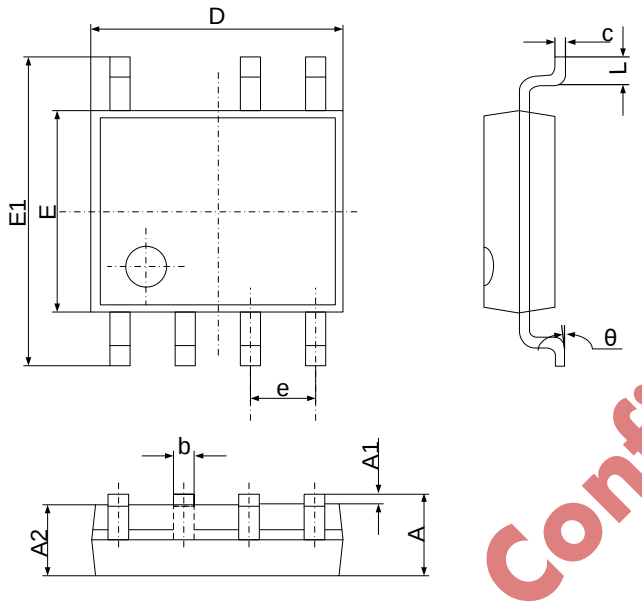
Top layer layout



Bottom layer layout

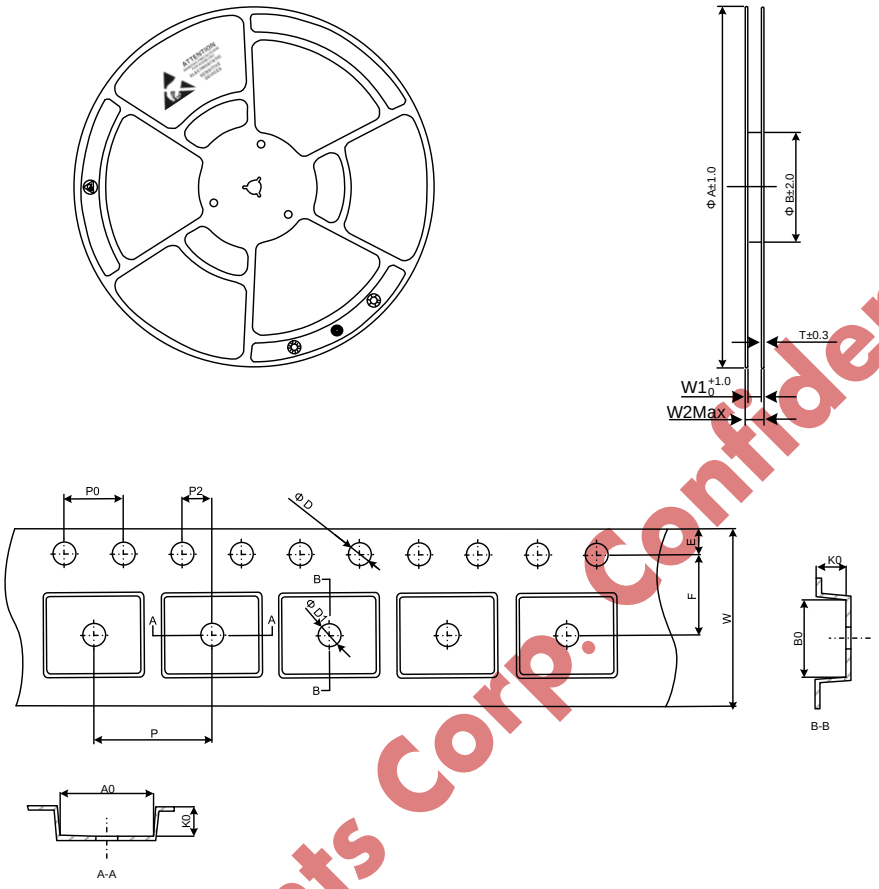
Package Dimension

SOP-7



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.300	1.500	0.051	0.059
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Tape and Reel Information



Reel Dimensions (mm)				
A	**B (Inner Diameter)**	**W1**	**W2Max**	**T**
330	100	12.4	18.4	1.5

Tape Dimensions			
Symbol	**Dimensions (mm)**	**Symbol**	**Dimensions (mm)**
E	1.75±0.10	W	12.00±0.10
F	5.50±0.10	P	8.00±0.10
P2	2.00±0.10	A0	6.60±0.10
D	$1.50^{+0.1}_{-0}$	B0	5.30±0.10
D1	1.55±0.05	K0	1.90±0.10
P0	4.00±0.10		

Packing Quantity				
Package	**Pcs/Reel**	**Reels/Box**	**Boxes/Carton**	**Pcs/Carton**
SOP-7	4000	2	8	64000

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